A MGy Radiation-Hardened Sensor Instrumentation SoC in a Commercial CMOS Technology

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***Abstract*— A radiation-hardened sensor instrumentation SoC is presented in this paper. The SoC is implemented in a standard CMOS technology, and achieves MGy-level TID radiation hardness through radiation-hardening-by-design. The SoC contains several commonly used analog/mixed-signal blocks (e.g., instrumentation amplifier, ADC, bandgap voltage reference, clock reference, multiplexer, etc.) in sensor readout systems. Circuit-level radiation-hardened-by-design techniques are introduced, and the effectiveness of these techniques is proven by on-line gamma-radiation assessments. Finally, implementation details of the sensor instrumentation SoC in a commercial 65nm CMOS technology are discussed.**

***Index Terms*—sensor instrumentation, signal conditioning, SoC, radiation-hardened-by-design, CMOS, instrumentation amplifier, delta-sigma, ADC, bandgap, total-ionizing-dose.**

I. Introduction

RECENT developments in the nuclear industry show an increasing demand for extremely radiation tolerant integrated circuits. Examples of these advanced nuclear applications are remote handling systems for the ITER (International Thermonuclear Experimental Reactor) fusion reactor to be built in Cadarache, France, LHC (Large Hadron Collider) at CERN and the MYRRHA (Multi-purpose Hybrid Research Reactor for High-tech Applications) reactor, which is being developed at SCK-CEN, Belgium. Beside these advanced nuclear installations there is also a growing need for complex robotic solutions that can withstand extreme radiation doses (>1MGy). Examples here are the remotely controlled interventions after the nuclear incident at Fukushima and the growing need for robotic nuclear reactor decommissioning solutions. All the aforementioned examples will benefit from electronic systems with MGy ionizing radiation tolerance.

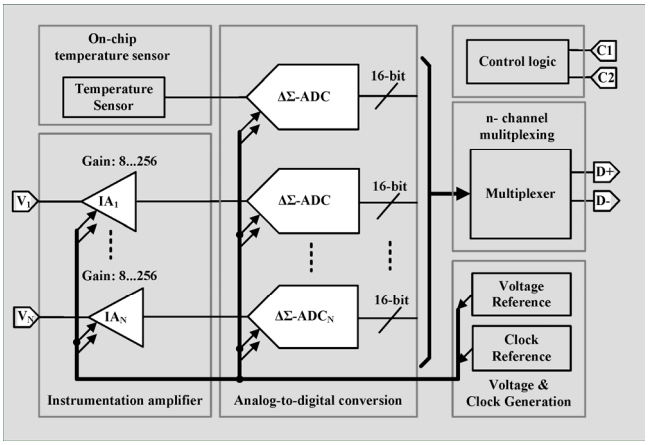

Fig. 1. System diagram of the sensor instrumentation SoC

Most of today's commercial off-the-shelf (COTS) electronics (Analog to Digital Converters (ADCs), amplifiers, voltage/clock references, multiplexers, etc.) are not specified to meet the demanding requirements of advanced nuclear applications requiring a MGy total ionizing dose tolerance [1]. They can only maintain their functionality in these radioactive environments through shielding with at least 10 centimeters of tungsten or lead. This leads to heavy and bulky solutions making the design, installation and replacement of these electronic solutions complex and expensive. Therefore the development of tailored MGy tolerant integrated solutions can present an advantage for use in these environments. It will not only reduce shielding but will make it possible to place electronics close to transducers and sensors in a radiation environment. This brings in several advantages. First, the analog signal from a transducer can be digitized close to the transducer. In this way, signal degradation over long cables to the control room through noise/interference can be avoided. Secondly, multiple sensor signals can be multiplexed digitally over a few signal wires. Hereby the number of cables is greatly reduced in the umbilical going to the control room. Thirdly, introduction of customized integrated circuits (IC) in these extreme environments allows for more advanced robotic or remote handling solutions, hence creating more degrees of

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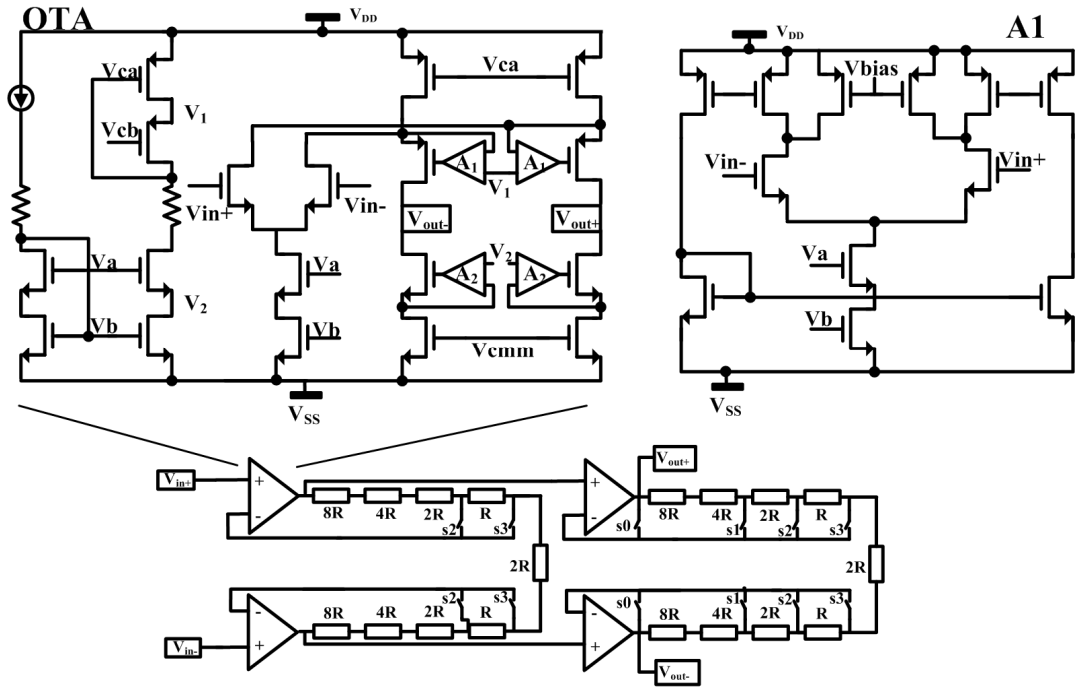

Fig. 2. Schematic of a radiation-tolerant SC instrumentation amplifier

TABLE I
SPECIFICATION OF THE SIGNAL CONDITIONING FRONTEND FOR READING OUT SENSORS

Sensor Type	RTD	Thermocouple	Strain	RDT/LVDT
F. S. input range (mV)	115	12	20	800
ADC resolution (bits)	12	12	12	16
IA Gain	8	64	40	1
Input noise (nV/√Hz@BW)	3500	367	500	15
Signal Bandwidth (Hz)	1	1	20	10k

freedom for system integrators.

As a mainstream integrated circuit fabricating process, commercial CMOS technology has been successfully implemented under ionizing radiation up to 1 MGy, demonstrated by customized radiation-tolerant IC applications at CERN [2]. Recent research also shows a trend in advanced CMOS technologies toward increased total dose hardness, due to downscaling of the CMOS gate oxide thickness [3]. This makes modern deep-submicron CMOS technology more suitable for radiation tolerant design. In this work, a complete sensor instrumentation SoC is implemented in a commercial advanced submicron CMOS technology. By employing radiation-hardened-by-design techniques on system, circuit, device and layout level, the SoC is able to achieve MGy-level radiation hardness, and at the same time, state-of-the-art performances which are comparable to non-rad-hard COTS components.

II. SENSOR INSTRUMENTATION SOC

The goal of the sensor instrumentation SoC (System-on-Chip) is to serve as an interface for reading out various common sensors, e.g., pressure sensors, thermocouples, RTDs and position sensors such as resolvers and LVDTs. This requires a universal signal conditioning SoC as shown in Figure 1. The SoC consists of N-channel programmable gain instrumentation amplifiers, N-channel delta-sigma ADCs, a multiplexer, an on-chip temperature sensor, a voltage reference and a clock reference. Among them, the instrumentation amplifier (IA) and the 16 bit ADC form a signal conditioning frontend, which is used to amplify small voltages coming from a pressure, displacement, temperature sensor or LVDT. The target specifications for the signal conditioning frontend of the Instrumentation SoC are shown in Table I.

The working principle of the instrumentation SoC is as follows: the gain of the frontend IA can be selected according to the sensor connected to the input. The RTD and LVDT don't require any amplification and will be directed to the ADC. The on-chip silicon temperature sensor provides a real time temperature measurement and can provide a temperature correction for the thermocouple. The digitized data of the sensors arrives in parallel at the different multiplexer inputs. The multiplexer is able to select the desired channel and to transform all the available signals at its input into a serial data stream. This data is then transferred together with the clock signal to a digital interface unit. The digital interface unit will translate the serial data stream into physical variables and provide additional conditioning. The angular value of the RDC will be recovered through a digital tracking loop [4]. In a

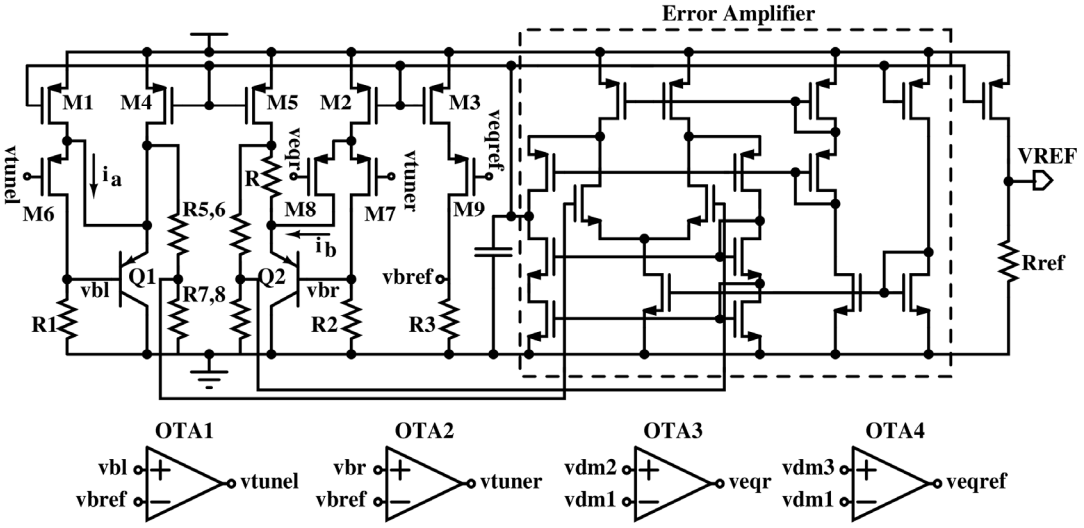

Fig. 3. Schematic of a radiation-hardened CMOS bandgap voltage reference

similar way the displacement of the LVDT will be read through a ratiometric principle.

Furthermore, a radiation tolerant clock reference will be necessary for the auto-zeroing amplifier inside the temperature sensor and the chopper-stabilization system of the instrumentation amplifier and the delta-sigma ADC. By implementing this clock reference on-chip, noise coupling to the clock signal through the long transmitting cable can thus be avoided. For the same reason, an on-chip radiation-hardened voltage reference is also required to provide a stable reference voltage for all functional blocks.

Major building blocks of the sensor instrumentation SoC have been implemented and assessed in 130 nm CMOS technology [5][6][7]. In this work, all individual components are integrated on the same chip, and the SoC will be implemented in 65nm CMOS technology. The main reason to choose the 65 nm CMOS technology is that it offers improved intrinsic TID radiation hardness [8], smaller geometry thus higher integration level, and higher operating frequencies.

III. Radiation-Hardened-by-Design Techniques

Over the course of the past decade, the TID radiation hardness of commercial CMOS technologies has been evolving rapidly, due to the continual shrinking of the gate-oxide thickness. However, there is no guarantee on the same radiation tolerance level among different processes at the same technology node provided by different manufacturers, since the radiation hardness is not a parameter that commercial semiconductor foundries monitor [1]. Therefore, besides choosing a more advanced CMOS technology for radiation-hardened designs, radiation-hardened-by-design (RHBD) techniques are also required in the circuit to ensure its reliability and performance even under an extreme radiation level. Two examples are given in this section to demonstrate the design strategy and effectiveness of the RHBD techniques.

A. RHBD Instrumentation Amplifier employing Chopper-Stabilization

Figure 2 shows the design of the instrumentation amplifier. The instrumentation amplifier has a programmable gain from 8 to 256. The OTA used in the instrumentation amplifier requires a high and stable gain to keep down the offset and gain drift as a function of temperature and radiation. Therefore a folded cascode stage with additional gain boosting through amplifiers A1 and A2 is used. Experiments at high radiation doses have emphasized the need to maintain the transistors' functionality. Therefore these amplifiers are configured so that they can cope with degradation of carriers mobility and variation of threshold-voltages.

Instead of inserting extra current to maintain the transconductance of the transistors, here a degradation of the transconductance (*gm*) is compensated by an increase in the output resistance of the gain boosting amplifiers A1 and A2. Degradation of mobility and/or threshold voltage is detected by a constant-gm current reference and fed through the current bleeding transistors of A1 by a certain ratio. Hereby the total gain of the OTA is kept reasonably high to not affect the gain and offset behavior of the instrumentation amplifier.

B. RHBD Voltage References with Dynamic Base Leakage Compensation

Another example is a radiation-hardened voltage reference. Although CMOS gate transistors fabricated in deep-sub-micron technology have shown excellent radiation tolerance, the diode still suffers from radiation induced leakage current [9]. A shallow trench isolation field oxide layer is usually placed surrounding the p+ diffusion region, which is the emitter of the pnp transistor. Radiation induced holes get trapped in the body of the field oxide near the SiO_2 – Si interface. This increases the base leakage current, and degrades the current gain of the bipolar transistor. Consequently, when the bipolar transistors are used in a bandgap voltage reference, the output voltage/current will

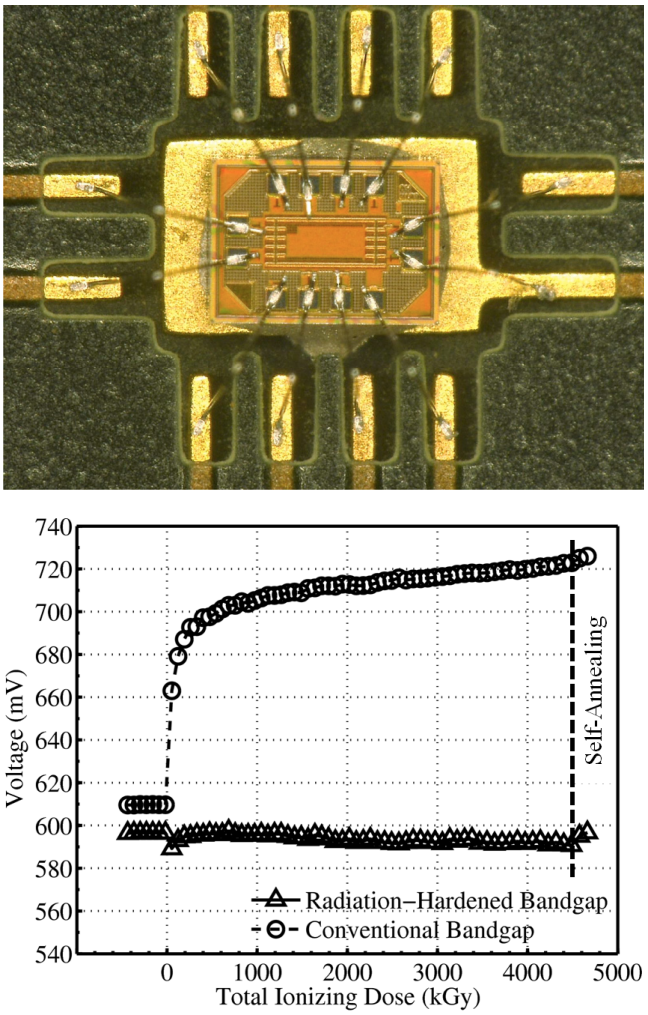

Fig. 4. Chip photo of a PCB-bonded bandgap reference after gamma irradiation and measured output voltages of the radiation-hardened bandgap reference and the conventional bandgap reference in 130nm CMOS

undergo dramatic changes.

A detailed explanation of this phenomenon can be found in [6]. A dynamic compensation technique can be employed to improve the radiation hardness of the conventional bandgap reference where only conventional CMOS diodes are used. The schematic is shown in Figure 3. The purpose of the dynamic compensation unit is to provide the base current for all the diodes. Therefore, only the collector current is flowing in the core circuits. According to early irradiation assessment results, the collector current of the diode is nearly unaffected by the increasing ionizing dose. The base leakage currents induced by irradiation will only flow through the compensation circuits, which keeps the bandgap current ID_{M5} and ID_{M4} constant.

C. Gamma-Radiation Assessment

Some of the blocks of the sensor instrumentation SoC has already been fabricated in 130 nm CMOS technology. The effectiveness of aforementioned RHBD techniques has also been demonstrated by gamma radiation assessment. As an example, one experiment was carried out in the "Brigitte"

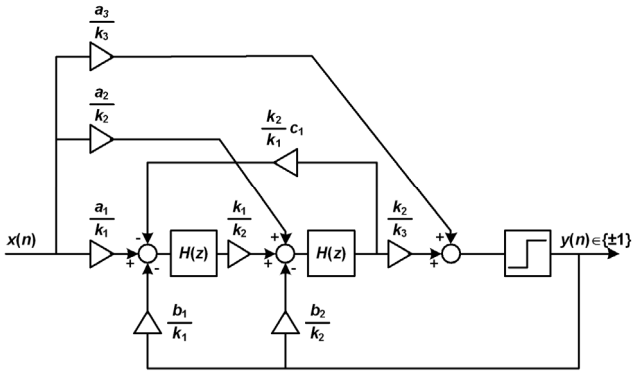

Fig. 5. Behavior model of the 2nd-order delta-sigma ADC

TABLE II
FEEDBACK AND SCALING COEFFICIENTS FOR THE CHOSEN NTF(Z)

Coefficient	Value	Coefficient	Value
a1	5.0	c1	2.8E-4
a2	18.0	k1	10.3
a3	23.3	k2	174.5
b1	5.0	k3	23.3
b2	18.0		

facility at the Belgium Nuclear Research Centre, SCK•CEN. Substrates bonded with both conventional and radiation-hardened bandgap references from the same technology run are irradiated with ^{60}Co gamma source. A high dose rate of 27 kGy/h is applied, which enables us to achieve a TID of 4.5 MGy in one week. As shown in Figure 4, the output reference voltage of the bandgap employing the DBLC technique stays consistent with the pre-rad value. A variation of only 1% is found from 0 to 4.5 MGy.

IV. IMPLEMENTATION IN 65NM CMOS AND SIMULATION RESULTS

The implementation of the sensor instrumentation SoC in 65 nm CMOS technology is a straight port of the 130 nm CMOS design. Although new design challenges arise in deep-sub-micron analog CMOS design era, such as increased gate leakage current and transistor output conductance, same RHBD techniques are still proving effective. The same instrumentation amplifier and bandgap voltage reference structures are thus used again in the 65 nm CMOS design. Specific details regarding design of other functional blocks (e.g., ADC, clock reference) in the 65 nm CMOS sensor instrumentation SoC are discussed in this section.

A. Delta-Sigma ADC

The ADC employed in the SoC is a single-loop 2nd-order 1-bit feed-forward Delta-Sigma modulator. The principle behavior model of the ADC is shown in Figure 5. The transfer function of *H(z)* in Figure 5 is $z^{-1}/(1-z^{-1})$. *H(z)* is an integrator with one sample delay. The coefficients, a1, a2 and a3 (called the feedforward coefficients) are used to cancel out the signal from the feedback at the input of each integrator, which greatly reduces the signal swing requirement of the integrators (since now only the quantization noise are needed to be

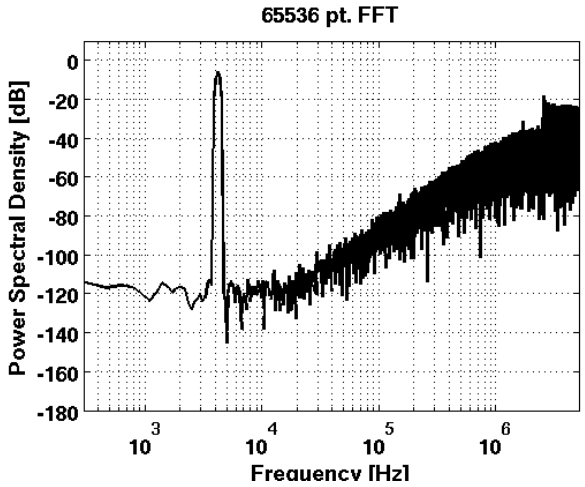

Fig. 6. Output power spectrum density of the delta-sigma ADC with -6dBFS input signal

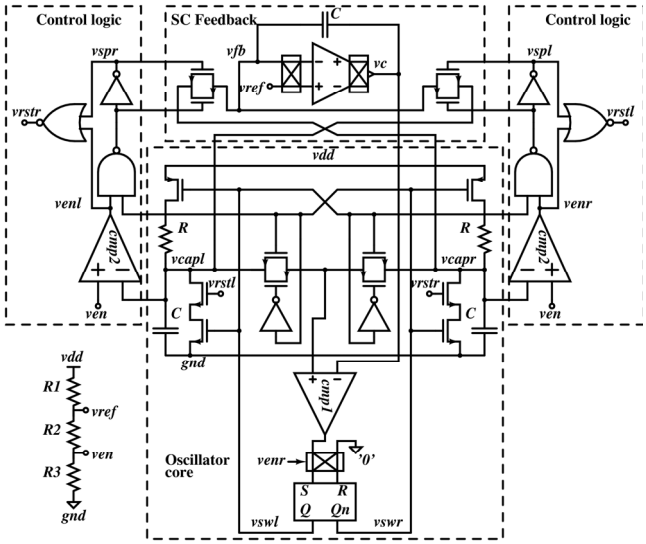

Fig. 7. Schematic of the on-chip RC oscillator with SC IEF

processed). The coefficients, b1 and b2 (called the feedback coefficients) are determined by the NTF(z). The coefficients, k1, k2, and k3 (called the scaling coefficients) are used to scale the signal swing at the output of the integrators. The coefficient c1 is used to optimize the zero's locations of the NTF(z). The coefficients for the chosen NTF(z) are listed in Table II. The converter has a bandwidth of 20 kHz and an oversampling ratio (OSR) of 256, which results in a sampling frequency of 10.24 MHz. The targeted resolution of the converter is 16 bits.

The ADC is simulated with an input signal of -6dBFS (full scale = 1.2 V) amplitude and a frequency of 4.22 kHz. The output spectrum is shown in Figure 6, from which one can calculate that an SNDR of 94dB and an ENOB of 16.1bit are achieved.

RHBD techniques have also been implemented to guarantee the radiation hardness of the ADC, such as: appropriate sizing of CMOS transistors to limit performance degradation

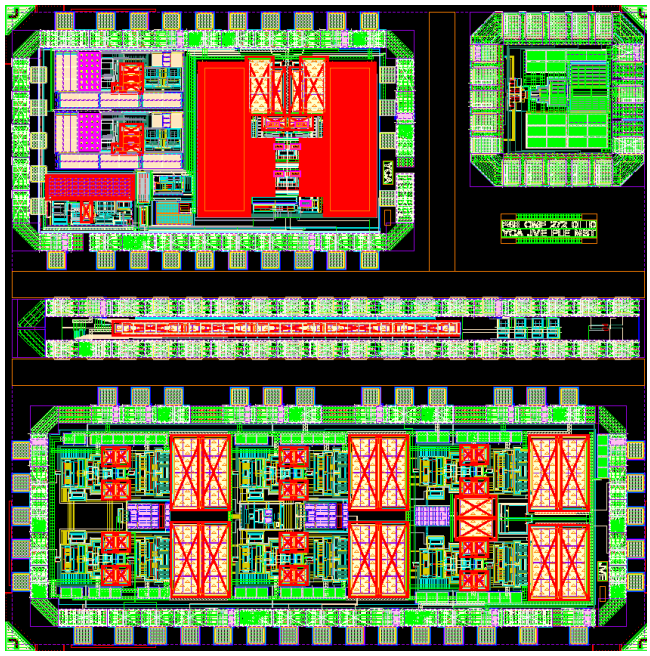

Fig. 8. Layout of the sensor instrumentation SoC in 65nm CMOS

introduced by TID radiation, employing radiation tolerant logic cells to avoid functional error caused by single-event effects, and implementing guard-ring structures to mitigate single-event latch-up.

B. On-Chip RC Oscillator

It is crucial to integrate an on-chip reference clock generator which provides clock signals to various functional blocks in the ADC, IA, and the temperature sensor, e.g., sample/hold circuits, chopper-stabilization circuits, and auto-zeroing circuits. Relaxation oscillators are suitable candidates to generate such reference clocks due to their compact size, low power consumption and wide frequency tuning range. However, the poor phase noise performance and large long-term variation are two major problems which limit their application.

Those issues can be solved by employing a switched-capacitor (SC) integrated error feedback (IEF) [10], as shown in Figure 7. The integrating operation is performed in a predefined integrate-and-hold (IH) phase *th*. This is realized by using only few additional control units. The main purpose of the control logic is to guarantee one capacitor is reset to '0' before the other reaches *vref*. Then, the alternate charging process can be sustained without being disrupted. This is secured by using a second comparator *cmp2* which has been set to a lower threshold *ven* to monitor the voltages at the capacitors. Once it crosses *ven*, the comparator generates a signal to terminate the integrating phase and turns the SC integrator into hold. Since *cmp2* is only used to produce clock signals for the IH circuits, its noise specification has no influence on the oscillator's overall phase noise.

The implemented oscillator in 65nm CMOS technology has an output frequency of 10.24 MHz. It achieves a phase noise of -60 dBc/Hz at 1 kHz offset frequency, and -122 dBc/Hz at 1

TABLE III
PERFORMANCE SUMMARY OF THE SENSOR INSTRUMENTATION SOC

Block	Parameter	Unit	Value	Block	Parameter	Unit	Value
IA	Gain	--	8 - 256	IA	Bandwidth	Hz	300
	PSRR	dB	100		CMRR	dB	110
	Supply voltage	V	1.2		Power consumption	mW	5.2
	Input noise	nV/√Hz	24		Offset drift	nV/ºC	10
ADC	ENOB	Bits	16	ADC	Bandwidth	Hz	20k
	Fsample	MHz	10		SNDR	dB	98
	Supply voltage	V	1.2		Power consumption	mW	3.4
Bandgap reference	VREF	mV	600	Bandgap reference	INL	mV	2
	Temperature coefficient	µV/ºC	30		Output drift (@1MGy)	%	0.2
	Supply voltage	V	1.2		Power consumption	µW	74
Clock reference	Frequency	MHz	10	Clock reference	Jitter	ps	25
	Temperature coefficient	%	±1 (from 0 to 80ºC)		Supply coefficient	%	±0.1 (from 1.1 to 1.5V)
	Supply voltage	V	1.2		Power consumption	mW	360
Temperature sensor	Temperature sensitivity	mV/ºC	1.5	Temperature sensor	INL	ºC	1
	Supply voltage	V	1.2		Power consumption	µW	56
Multiplexer	Data rate	MHz	16	Multiplexer	Supply voltage	V	1.2
	Input impedance	Ω	100		Output impedance	Ω	50

MHz offset frequency. The simulated cycle jitter (Jc) is 25 ps.

C. System Integration

In order to ease the test setup for the instrumentation SoC, all functional blocks were grouped into three separate pad-ring structures, but all were located on the same die. As illustrated in Figure 8, the instrumentation amplifier is located at the bottom of the die, and the multiplexer is situated on the top-right corner of the system, whereas all other blocks are located on the top-left corner. A brief description of the performance of all functional blocks is given in Table III.

V. CONCLUSION

A MGy TID radiation tolerant sensor instrumentation SoC has been described in this paper. It integrates several critical functional blocks on the same chip to read out various common sensors in a hazardous radiation environment. This configuration greatly eases the implementation of remote handling systems in nuclear reactors. The chip is designed in a commercial standard 65 nm CMOS technology. RHBD techniques are applied to achieve MGy TID radiation tolerance, which ensures the reliability of the electronic systems.

VI. DISCLAIMER

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